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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
UMEZ ERONINI, LYNETTE T	
ART UNIT	PAPER NUMBER
1765	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/797,188	EMA ET AL.	
	Examiner	Art Unit	
	Lynette T. Umez-Eronini	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *2 and 5* is/are allowed.

6)☒ Claim(s) *1,3 and 6-19* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *3/11/04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114 to reconsider the rejection of the claims over the formerly applied references. Applicant's submission filed on 10/14/2006 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1, 3, 4, 15, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shono et al. (US 5,365,095) in view Minami (US 4,252,840).

Shono teaches, a method for fabricating a semiconductor device comprising the steps of:

forming a conductor pattern **6** over a semiconductor substrate **1** (column 7, lines 57-61);

forming a first insulation film **10** covering the conductor pattern (column 7, line 66-column 8, line 2);

forming over the first insulation **10** film a second insulation **13** film (column 8, lines 17-22);

forming over the second insulation film **13** a third insulation film **15** (column 28-33);

forming over the third insulation film a mask layer (column 8, lines 37-41);

forming a hole **18** in the third insulation film **10**, the second insulation film **13** and the first insulation film **15** (column 8, lines 62-68);

the second insulation film **13** being (250 nm and 450 nm) thinner than the third insulation film **15** (1600 nm), (column 7, line 66 - column 8, lines 2 and 17-19); and

the step of forming the hole including a first step of etching the third insulation, a second step of etching the second insulation film, and a third step of etching the first

insulation film; an etching condition at the first step being different form that at the second step, **in claim 1**; and

in the third step, the opening is opened down to semiconductor substrate, **in claim 3**; and

Shono differs in failing to teach forming over the first insulation layer a second insulation film having etching characteristics different from those of the first insulation film;

forming over the second insulation film a third insulation film having etching characteristics different from those of the second insulation film; and

the step of forming the hole including a first step of etching the third insulation film, a second step or etching the second insulation film and a third step of etching the first insulating film, an etching condition at the first step being different from that at the second step, **in claim 1**;

wherein in the step of forming the hole, an etching rate of the second insulation film at the first step is lower than an etching rate of the third insulation film at the first step and an etching rate of the second insulation film at the second step, **in claim 15**; and

in the first step, the insulation film is etched with the second insulation film as a stopper, **in claim 19**.

Minami teaches first, second and third insulating layers **7, 10, and 11** are made of different materials and etched at different rates (column 2, line 55 - column 3, line 10 and 20-22). The aforementioned also reads on a second insulation film having etching

characteristics different from those of the first insulation film and a second insulation film a third insulation film having etching characteristics different from those of the second insulation film and an etching condition at the first step being different form that at the second step, **in claim 1**. Further, Minami's method of etching suggests each insulating layer is etched individually, therefore, Minami's etching method reads on, wherein in the step of forming the hole, an etching rate of the second insulation film at the first step is lower than an etching rate of the third insulation film at the first step and an etching rate of the second insulation film at the second step, **in claim 15**. Also, the above aforementioned suggests the third insulation film is etched with the second insulation film as a stopper, **in claim 19** because an etch stop layer is an underlying material that has different etch characteristics than an overlying material to be etched.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Shono by using Minami's method of etching insulating layers because such method is used in a method of manufacturing semiconductor device with good yield and in the highly integrated form (column 1, lines 33-35).

5. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shono (US '095) in view Minima (US '840) and further in view of Dennison et al. (US 5,338,700).

Shono in view of Minima teaches all of the limitations as in re claim 1. Shono also teaches, ion diffused layer **2** composed of drain **3** and on the p-type semiconductor

substrate **1** (same as Applicants' impurity doped region in a semiconductor substrate), (column 3, lines 57-60 and FIG. 3(a)).

Shono in view of Minima differs in failing to teach polishing the second insulation film, **in claim 6** and polishing the second film by chemical mechanical polishing, **in claim 7**.

Dennison discloses providing planarized insulating material (column 2, lines 52-55 and 61-63)"a planarized layer **28** such as BPSG . . ." (column 3, lines 34-36) and ". . . planarized first layer **28** of an insulating material . . . which is planarized back by chemical mechanical polishing (CMP)" (column 3, lines 50-54).

Since Dennison illustrates forming a planarized insulation film by chemical mechanical polishing is known, then it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Shono in view of Minima by planarizing an insulation layer as taught in the Dennison reference because planarizing an insulation layer is known to be effective in fabricating semiconductor devices having a bit line over capacitor (column 1, lines 19-column 2, lines 42-55) over conventional capacitors with buried bit line construction.

6. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shono (US '095) in view Minima (US '840) and further in view of Dennison (US '700).

Shono in view Minima teach all of the limitations as in re claim 1.

Shono in view Minima differs in failing to teach polishing the second insulation film, **in claim 12** and polishing the second film by chemical mechanical polishing, **in claim 13**.

Dennison discloses providing planarized insulating material (column 2, lines 52-55 and 61-63) "a planarized layer **28** such as BPSG . . ." (column 3, lines 34-36) and ". . . planarized first layer **28** of an insulating material . . . which is planarized back by chemical mechanical polishing (CMP)" (column 3, lines 50-54).

Since Dennison illustrates forming a planarized insulation film by chemical mechanical polishing is known, then it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Shono in view Minima by planarizing an insulation layer as taught in the Dennison reference because planarizing an insulation layer is known to be effective in fabricating semiconductor devices having a bit line over capacitor (column 1, lines 19-column 2, lines 42-55) over conventional capacitors with buried bit line construction.

7. Claims 8 and 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Shono (US '095) in view of Minima (US 840) and Dennison (US '700) of as applied respectively to claims 6 and 12 above, and further in view of Goth et al. (US 4,758,528).

Shono in view of Minima and Dennison differs in failing to teach each of the first insulation film and the third insulation film is formed of silicon nitride, and each of the second insulation film and the fourth insulation film is formed of doped silicon oxide.

Goth teaches discloses an insulating layer can be any one of several conventional insulators or combination of insulators such as silicon dioxide (same as

Applicants' undoped oxide), silicon nitride, etc. (column 6, line 67 - column 7, lines 1-4 and 32-36).

Since Goth illustrates an insulating layer comprising silicon nitride and silicon dioxide (same as Applicants' undoped oxide) is known, then it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Shono in view of Minima and Dennison by using conventional insulators as taught by Goth because insulators are used in a method of making narrowed dimensioned dielectric to provide for structures having less than 1 micron (Abstract).

Allowable Subject Matter

8. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: As to claim 4, the prior art of record taken alone or in combination fails to suggest, teach or render obvious wherein the third step of etching the first insulation film, the opening is opened to the conductor pattern, along with the limitations of any of the intervening claims.

10. Claims 2 and 5 are allowed.

11. The following is an examiner's statement of reasons for allowance:

As to claims 2 4, and 5, the prior art of record taken alone or in combination fails to suggest, teach or render obvious a method for fabricating the semiconductor device, as defined the steps of the claim;

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

12. Applicants' arguments with respect to claims 1, 3, 4, and 15 have been considered but are moot in view of the new ground(s) of rejection because the formerly applied references failed to address "A method for fabricating a semiconductor device comprising . . . the second insulation film being thinner than the third insulation film, in (Currently Amended) Claim 1.

13. Applicants' arguments see Remarks, filed 10/12/2006, with respect to claims 6-14, and 17-18 have been fully considered and are persuasive. The rejection of claims 6-14 under 35 U.S. C. 102(e) as being anticipated by and the rejection of claims 6 (should have read "16"), 17, and 18 under 35 U.S.C. §103(a) over Ema et al. (US 6,744,091) has been withdrawn because the Ema (US '091) reference is a (09/637,356) divisional of a prior application 09/037,068), thereby disqualifying as prior art under 35 U.S.C.§ 102(e).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynette T. Umez-Eronini whose telephone number is 571-272-1470. The examiner is normally unavailable on the First Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Art Unit 1765

ltue

December 19, 2006

GREGORY MILLS
SUPERVISORY PATENT EXAMINER
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